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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,098	12/21/2000	Nicholas J. Kelsey	20880-05093; Case 5093	4360

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EXAMINER	
HARKNESS, CHARLES A	
ART UNIT	**PAPER NUMBER**
2183	7

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,098	KELSEY ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 21 December 2000 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 December 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Information Disclosure Statement as received on 06/14/01; Declaration Fee as received on 07/10/01; and PreAmendmeant as received on 10/07/02.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-9, and 13-15 is rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al, U.S. Patent Number 6,317,774 (herein referred to as Jones).

5. Referring to claim 1 Jones has taught a computer based system for switching between program contexts comprising:

An embedded pipelined processor (Jones column 4 lines 49-52; since the processor supports embedded constraints, it would be an embedded processor) capable having a first program thread and a second program thread in an execution pipeline

(Jones column 1 lines 12-16; this is the description of a multitasking, or multithreading, processor or system);

A first set of data storage devices capable of storing a first state of said embedded processor (Jones column 1 lines 18-37, column 6 lines 28-43; each thread has its own data structure which is stored in memory, each one containing status information);

A second set of data storage devices capable of storing a second state of said embedded processor (Jones column 1 lines 18-37, column 6 lines 28-43; each thread has its own data structure which is stored in memory, each one containing status information); and

A thread scheduler for identifying which of said program threads said embedded processor executes (Jones column 6 lines 28-44, figure 1, reference 32);

Wherein said processor switches between said first and second state in a time period between the end of the execution of a first program instruction in the first thread and the beginning of the execution of a second program instruction in the second thread (Jones column 6 lines 28-44, figure 1, reference 32; the normal operation of a switch between threads would occur in the order of the current thread finishing execution, and saving its status, bring in the next threads context information and then begin execution of the new thread; the processor cannot perform a context switch until the current thread is completed its execution, otherwise the current thread will not be saved).

6. Referring to claim 2 Jones has taught wherein said first state is the state of the embedded processor during the execution of the first program thread Jones column 1 lines 18-37, column 6 lines 28-43; each thread has its own data structure which is stored in memory, each one containing status information).

7. Referring to claim 3 Jones has taught wherein said second state is the state of the embedded processor during the execution of the second program thread (Jones column 1 lines 18-37, column 6 lines 28-43; each thread has its own data structure which is stored in memory, each one containing status information).

8. Referring to claim 5 Jones has taught wherein said thread scheduler includes:

A thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread (Jones column 4 lines 27-57, figure 28 looking at threads 11-13, some threads are shown as guaranteed and some are not; although Jones does not explicitly call the real time thread a "hard real time" thread, the way it is described is that the thread is guaranteed to be operated on and certain processor time, which is what is required of a hard real time thread, therefore including a hard real time thread by definition);

A HRT scheduler for regularly scheduling said HRT thread in available time quanta such that said HRT thread is scheduled to ensure the execution of the HRT in a predetermined time (Jones column 4 lines 42-57).

9. Referring to claim 6 Jones has taught wherein said time quanta is at least one instruction cycle (Jones column 4 lines 27-57, figure 28, the figure shows time greater than 1 cycle for each thread).

10. Referring to claim 7 Jones has taught wherein said thread scheduler schedules a non-real-time (NRT) thread to replace a scheduled HRT thread if said HRT is complete (Jones column 19 lines 22-34).

11. Referring to claim 8 Jones has taught wherein said thread scheduler schedules the execution of non-real-time (NRT) threads in quanta not allocated to HRT threads (Jones

column 19 lines 22-34, column 4 lines 27-57, figure 28; any time that is allocated that does not go to the hard real time threads must go to the non real time threads, because they are the only other threads available, and cannot be allocated at the same times as the HRTs).

12. Referring to claim 9 Jones wherein said thread scheduler regularly schedules NRT threads to be executed (Jones column 4 lines 52-57, column 16 line 55-column 17 line 11; since Jones teaches scheduling non real time threads at the same time as the real time threads, and also when no real time threads are present, the non real time threads are scheduled regularly; also the non real time threads are apart of all the queues of the round robin scheme, therefore being called upon on a regular basis).

13. Referring to claim 13 Jones has taught wherein said embedded processor is capable of restoring said second state of said embedded processor during execution of said first program thread (Jones column 16 lines 34-41; Jones shows where the context information is a queue and has been accepted for scheduling but is not yet executing, therefore it has been brought from memory while another thread is executing).

14. Referring to claim 14 Jones has taught wherein said embedded processor is capable of storing said second state of said embedded processor during execution of said first program thread (Jones column 1 lines 18-37, column 6 lines 28-43; since the other threads are already stored while the current thread is being executed, they can continue to sit in memory storage while the current thread is executing).

15. Referring to claim 15 Jones has taught wherein said first set of data storage devices comprises registers shared by a plurality of threads (Jones column 1 lines 17-37;

one of the threads context states will be loaded into the registers or stack at a time, so the registers that are shared can contain one of the context states of one of the threads).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of Borkenhagen et al, U.S. Patent Number 6,567,839 (herein referred to as Borkenhagen).

17. Referring to claim 4 Jones has not taught wherein said processor switches between said first and second states by changing a state selection register. Borkenhagen has taught wherein said processor switches between said first and second states by changing a state selection register (Borkenhagen column 16 lines 38-49). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a register to change the threads of a multithreaded system. The system of Jones must have some mechanism to control the thread switch, but does not disclose details of this logic. Borkenhagen does disclose a particular embodiment for this logic and states reasoning to use this type of switching logic for such reason as assigning certain threads priority, which ties into the Jones system which has hard real time threads (Borkenhagen abstract, column 5 line 66-column 6 line 11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to Borkenhagen to use a

register to change the threads of a multithreaded system if they want to do a detailed design since Jones does not describe that logic function.

18. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of Gutgold et al., U.S. Patent Number 6,026,503 (herein referred to as Gutgold).

19. Referring to claim 10 Jones has not taught wherein a first storage device for storing program instructions, said processor fetching instructions from the first storage device within a first fetch period;

A second storage device for storing program instructions, said processor fetching instructions from the second storage device within a second fetch period;

Wherein said first fetch period is substantially shorter than said second fetch period.

Gutgold has taught wherein a first storage device for storing program instructions, said processor fetching instructions from the first storage device within a first fetch period;

A second storage device for storing program instructions, said processor fetching instructions from the second storage device within a second fetch period;

Wherein said first fetch period is substantially shorter than said second fetch period (Gutgold column 3 lines 1-19; it is well known in the art that flash memory is not as fast in operation as RAM memory, therefore having a slower fetch period than that of the RAM memory fetches).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use two different memories to fetch instructions from. Gutgold has taught storing the debug executable information in the EEPROM, or ROM, and that having a debug mode

for a processor is beneficial since it allows the user to test the code they have written just as programmers test code on an emulator (Gutgold column 1 lines 27-45 and column 2 lines 20-26). By being able to test the code, the user can make sure the code runs efficiently and correctly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be able to debug the program code just as an emulator would, allows the program to be tested to make sure that is correct and does not causes errors.

20. Referring to claim 11 Jones and Gutgold has taught wherein said first storage device for storing program instructions comprises a static RAM (Gutgold column 3 lines 1-19).

21. Referring to claim 12 Jones and Gutgold has taught wherein said second storage device for storing program instructions comprises a flash memory (Gutgold column 3 lines 1-19).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

"Dynamic Scheduling of Hard Real-Time Tasks and Real-Time Threads", Schwan et al., has taught scheduling of Hard Real Time threads in a processor.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

October 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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